

Stacked device structures for resistive memory and logic

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Elektronische Materialien (PGI-7)

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Schriften des Forschungszentrums Jülich
Reihe Information / Information

Band / Volume 20

ISSN 1866-1777

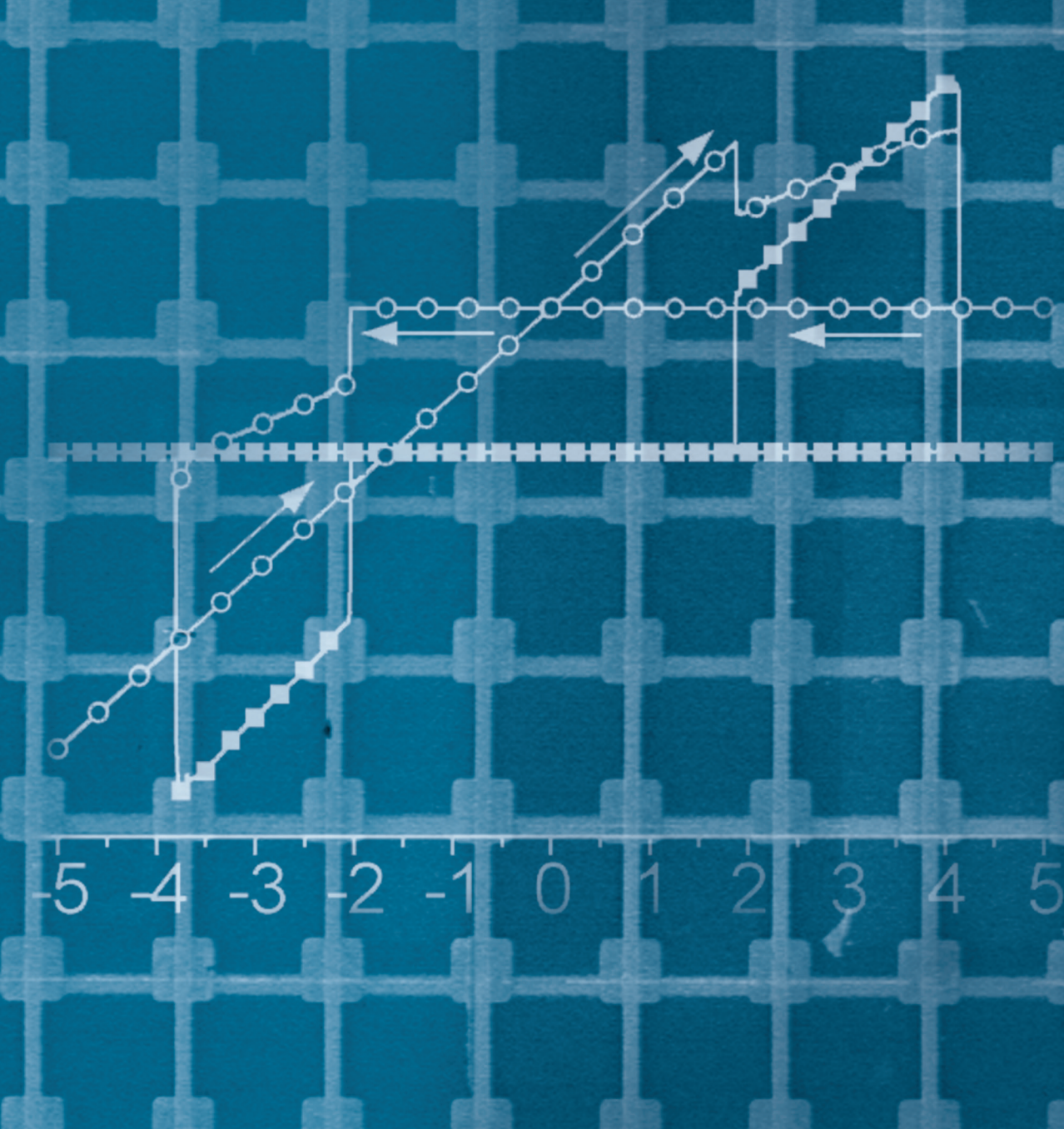
ISBN 978-3-89336-777-1

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ISBN 978-3-89336-777-1