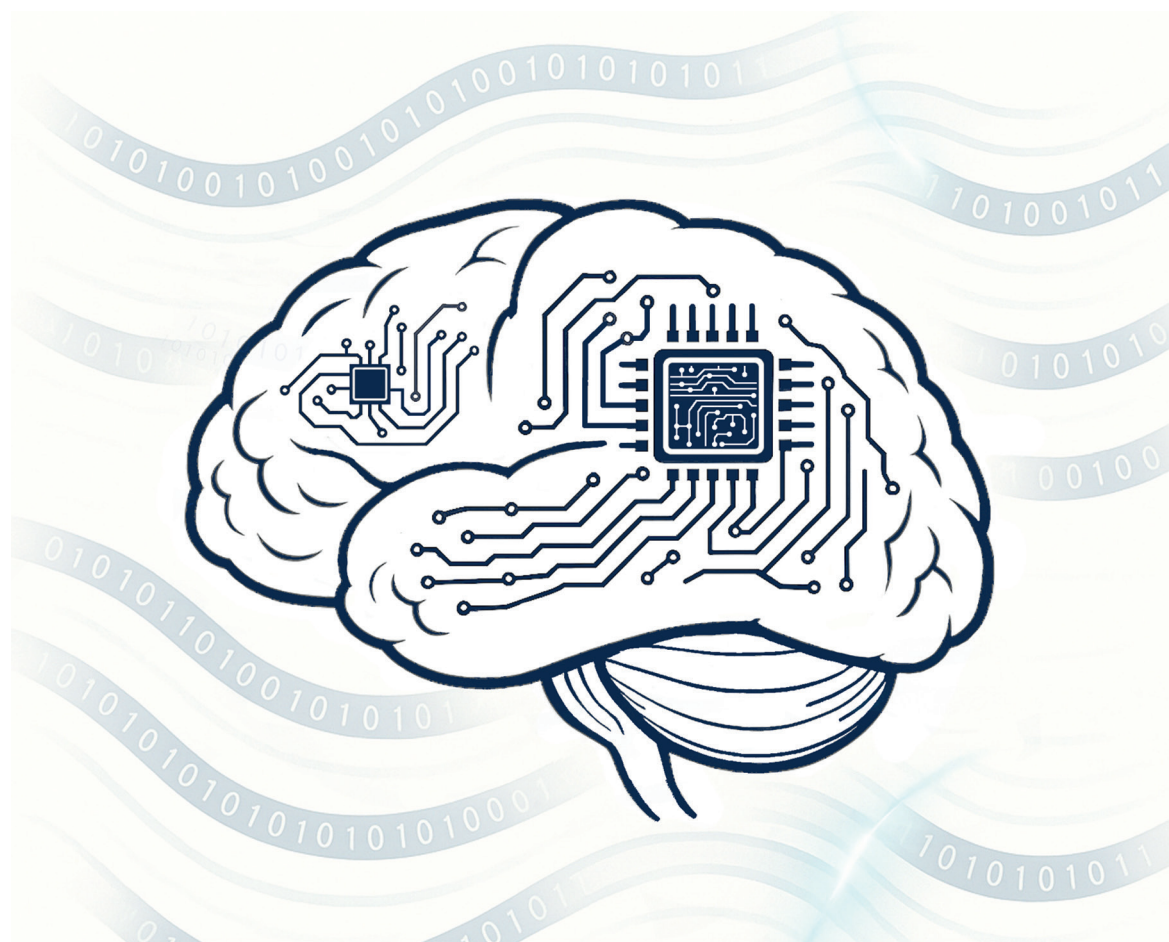




Development and Evaluation of Architecture Concepts for a System-on-Chip Based Neuromorphic Compute Node for Accelerated and Reproducible Simulations of Spiking Neural Networks in Neuroscience

Guido Trench

IAS Series

Band / Volume 71

ISBN 978-3-95806-832-2

Forschungszentrum Jülich GmbH
Institute for Advanced Simulation (IAS)
Jülich Supercomputing Centre (JSC)

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Schriften des Forschungszentrums Jülich
IAS Series

Band / Volume 71

ISSN 1868-8489

ISBN 978-3-95806-832-2

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